IN THE SPECIFICATION:

Please replace paragraph 19 with the paragraph below showing changes.

The system 100 includes a graph generator 110. The graph generator 110 parses a Hardware Description ~~High-level Design~~ Language (HDL) file 105, which may be a Verilog HDL file. HDL tools and the files they produce are well known to those skilled in the pertinent art. In the illustrated embodiment, the HDL file 105 is produced by a particular hardware description tool called "OTUS." Of course, other HDL file generating tools fall within the broad scope of the present invention. Table 1, below, illustrates an exemplary OTUS microprocessor interface hardware description language file that can be the HDL file 105.